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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,368	HAMAMOTO ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Introduction

1. Claims 46-54 of the application are pending.

Foreign Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application 02-181402 dated July 11, 1990, application 02-208072 dated August 8, 1990, application 03-057972 dated February 27, 1991 and application 03-057930 dated February 28, 1991 filed in Japan. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), as part of prior application Serial No. 07/727,420. The Applicant is required to submit certified copies of English translations of the above papers.

Continuing Application

3. Acknowledgment is made of the Applicant's request to treat this application as a continuation of Application 07/727,420 dated July 9, 1991and Application 08/446,278 dated May 22, 1995.

Information Disclosure Statement

4. Acknowledgment is made of the information disclosure statements filed on June 22, 2001 and January 28, 2002 together with copies of the papers and patents. The papers and patents have been considered in reviewing the claims.

Applicants have provided four untranslated Japanese office actions. They have been considered to the extent of the examiner's ability. It is suggested that the applicants submit an English translation to the examiner for a thorough consideration.

Drawings

5. Acknowledgment is made of the eighteen sheets of drawings submitted with the preliminary amendment with proposed corrections highlighted. The drawings are objected to as the under 37CFR 1.84(l) ads the lines, numbers and letters are not uniformly thick and well defined.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claim 46 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,282,611 and Claim 1 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the memory apparatus of Claim 46 is same as the memory card specified in Claim 1 of '611 and '431. All the elements of Claim 46 are covered in Claim 1 of '611.

8. Claim 47 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 3 of U.S. Patent No. 6,282,611 and Claim 6 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the communication means of Claim 47 is same as the communication channel specified in Claim 3 of '611 and Claim 6 of '431. All the elements of Claim 47 are covered in Claims of '611 and '431.

9. Claim 48 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 13 of U.S. Patent No. 6,282,611 and

Claim 13 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the built-in playback circuit of Claim 48 is same as the built-in playback circuit specified in Claim 13 of '611 and Claim 13 of '431. All the elements of Claim 48 are covered in Claims of '611 and '431.

10. Claim 49 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 12 of U.S. Patent No. 6,282,611 and Claim 12 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the memory apparatus of Claim 49 is same as the memory card specified in Claim 12 of '611 and Claim 12 of '431. All the elements of Claim 49 are covered in Claims of '611 and '431.

11. Claim 50 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 14 of U.S. Patent No. 6,282,611 and Claim 14 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the playback circuit of Claim 50 is same as the memory apparatus specified in Claim 14 of '611 and Claim 14 of '431. All the elements of Claim 50 are covered in Claims of '611 and '431.

12. Claim 51 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 14 of U.S. Patent No. 6,282,611 and

Claim 14 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the memory apparatus of Claim 50 is same as the memory card specified in Claim 10 of '611 and Claim 10 of '431. All the elements of Claim 51 are covered in Claims of '611 and '431.

12. Claim 51 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 14 of U.S. Patent No. 6,282,611 and Claim 14 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the memory apparatus of Claim 50 is same as the memory card specified in Claim 10 of '611 and Claim 10 of '431. All the elements of Claim 51 are covered in Claims of '611 and '431.

13. Claim 52 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 13 of U.S. Patent No. 6,282,611 and Claim 13 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the built-in playback circuit of Claim 48 is same as the built-in playback circuit specified in Claim 13 of '611 and Claim 13 of '431. All the elements of Claim 52 are covered in Claims of '611 and '431.

14. Claim 53 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 12 of U.S. Patent No. 6,282,611 and

Claim 12 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the memory apparatus of Claim 53 is same as the memory card specified in Claim 12 of '611 and Claim 12 of '431. All the elements of Claim 539 are covered in Claims of '611 and '431.

15. Claim 54 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 14 of U.S. Patent No. 6,282,611 and Claim 14 of U.S. Patent No. 2001/0037431. Although the conflicting claims are not identical, they are not patentably distinct from each other because the playback circuit of Claim 54 is same as the memory apparatus specified in Claim 14 of '611 and Claim 14 of '431. All the elements of Claim 50 are covered in Claims of '611 and '431.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

17. Claims 46 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Nomura et al. (NO)** (U.S. Patent 4,779,138) further in view of **Jinguji (JI)** (U.S. Patent 4,847,840) and **Kramer (KR)** (U.S. Patent 4,991,218).

17.1 **KKR** teaches a portable data processing and storage system. Specifically, as per Claim 46, **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source. (Col 1, Line 61 to Col 2, Line 9). **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to reproduce the digital data stored therein independently of the digital signal source. (Col 1, Line 61 to Col 2, Line 9).

KKR does not expressly teach that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source. **NO** teaches that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source. (Col 11, Line 65 to Col 12, Line 18). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the memory apparatus of **KKR** with the memory apparatus having a built-in memory circuit formed of a semiconductor memory of **NO**, as the semiconductor memory is fast and small.

KKR teaches that the memory apparatus has a built-in playback circuit. **KKR** does not expressly teach that the memory apparatus has a built-in playback circuit, including a digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in the memory circuit. **JI** teaches that the memory apparatus has a built-in playback circuit, including a digital-to-analog converter and a filter circuit for reproducing digital data stored in the memory circuit. (Fig. 19; Col 4, Lines 6-9 and Col 12, Lines 53-59). It would have

been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with digital-to-analog converter and a filter circuit of **JI**, since all playback circuits require the digital-to-analog converter and a filter circuit.

KKR does not expressly teach that the memory apparatus has a built-in playback circuit, including an audio amplifier, for reproducing digital data stored in the memory circuit. **KR** teaches that the memory apparatus has a built-in playback circuit, including an audio amplifier for reproducing digital data stored in the memory circuit. (Fig. 1; Col 9, Lines 10-12). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with audio amplifier of **KR**, since that would provide varying amplification of the output audio.

17.2 As per Claim 48, **KKR** does not expressly teach that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. **JI** teaches that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. (Col 12, Lines 63-67). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with identification (ID) code of **JI**, since that would facilitate selecting various options based on the identification code.

17.3 As per Claim 49, **KKR** teaches that the memory apparatus is a card-like storage medium. (Col 1, Line 61 to Col 2 Line 9).

17.4 As per Claim 50, **JI** teaches that the playback circuit has playback conditions which include stereo or monaural playback (Col 12, Lines 43-45; Col 12 Line 67 to Col 13 Line 5), and a sampling frequency. (Col 13, Lines 6-16 and Col 13 Lines 28-39).
KKR does not expressly teach that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. **KR** teaches that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. (Col 5, Lines 5-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with playback conditions which include a resolution of 8 and 16 bits of **KR**, since that would provide different resolutions of the output audio signal.

18. Claims 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al.** (**KKR**) (U.S. Patent 4,667,0880) in view of **Nomura et al.** (**NO**) (U.S. Patent 4,779,138), **Jinguji** (**JI**) (U.S. Patent 4,847,840), and **Kramer** (**KR**) (U.S. Patent 4,991,218) further in view of **Ukegawa** (**UK**) (U.S. Patent 4,926,463).

18.1 As per Claim 47, **KKR** does not expressly teach that the digital data is transmitted by communication means. **UK** teaches that the digital data is transmitted by communication means. (Col 2, Line 64 to Col 3 Line 7). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with communication means of **UK**, since that would facilitate reception of the audio programs from the audio source at remote locations through the communication means.

19. Claims 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Nomura et al. (NO)** (U.S. Patent 4,779,138) further in view of **Jinguji (JI)** (U.S. Patent 4,847,840), **Kramer (KR)** (U.S. Patent 4,991,218) and **Tarlow et al. (TA)** (U.S. Patent 5,045,327).

19.1 As per Claim 51, **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source. (Col 1, Line 61 to Col 2, Line 9). **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to reproduce the digital data stored therein independently of the digital signal source. (Col 1, Line 61 to Col 2, Line 9).

KKR does not expressly teach that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source. **NO** teaches that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source. (Col 11, Line 65 to Col 12, Line 18). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the memory apparatus of **KKR** with the memory apparatus having a built-in memory circuit formed of a semiconductor memory of **NO**, as the semiconductor memory is fast and small.

KKR teaches that the memory apparatus has a built-in playback circuit. **KKR** does not expressly teach that the memory apparatus has a built-in playback circuit, including a

digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in the memory circuit. **JI** teaches that the memory apparatus has a built-in playback circuit, including a digital-to-analog converter and a filter circuit for reproducing digital data stored in the memory circuit. (Fig. 19; Col 4, Lines 6-9 and Col 12, Lines 53-59). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with digital-to-analog converter and a filter circuit of **JI**, since all playback circuits require the digital-to-analog converter and a filter circuit.

KKR does not expressly teach that the memory apparatus has a built-in playback circuit, including an audio amplifier, for reproducing digital data stored in the memory circuit. **KR** teaches that the memory apparatus has a built-in playback circuit, including an audio amplifier for reproducing digital data stored in the memory circuit. (Fig. 1; Col 9, Lines 10-12). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with audio amplifier of **KR**, since that would provide varying amplification of the output audio.

KKR does not expressly teach that the memory apparatus has a rechargeable battery capable of being charged by a power supply in the digital signal source when the memory card is connected with the digital signal source. **TA** teaches that the memory apparatus has a power supply battery. (Col 2, Lines 39-40). Official notice is taken that the battery could be capable of being charged by a power supply in the digital signal source when the memory card is connected with the digital signal source. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with rechargeable battery of **TA**, since that would facilitate using the memory apparatus with portable devices.

19.2 As per Claim 52, **KKR** does not expressly teach that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. **JI** teaches that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. (Col 12, Lines 63-67). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with identification (ID) code of **JI**, since that would facilitate selecting various options based on the identification code.

19.3 As per Claim 53, **KKR** teaches that the memory apparatus is a card-like storage medium. (Col 1, Line 61 to Col 2 Line 9).

19.4 As per Claim 54, **KKR** does not expressly teach that the playback circuit has playback conditions which include stereo or monaural playback and a sampling frequency. **JI** teaches that the playback circuit has playback conditions which include stereo or monaural playback (Col 12, Lines 43-45; Col 12 Line 67 to Col 13 Line 5), and a sampling frequency. (Col 13, Lines 6-16 and Col 13 Lines 28-39). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with playback conditions which include stereo or monaural playback and a sampling frequency of **JI**, since that would provide different selection options for the output audio signal.

KKR does not expressly teach that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. **KR** teaches that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. (Col 5, Lines 5-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the built-in playback circuit of **KKR** with playback conditions which include a resolution of 8 and 16 bits of **KR**, since that would provide different resolutions of the output audio signal.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
April 1, 2002

DR. HUGH M. JONES
PATENT EXAMINER
ART UNIT 2123